In the Specification:

Please amend paragraph 0007 as follows:

An aspect of the present invention provides a vertical dynamic random access memory (DRAM) cell device fabricated within a trench region in a substrate, the trench having first and second opposing substantially vertical edges. The vertical DRAM cell comprises a storage capacitor formed within the trench region for storing electrical charge, a transistor formed within the trench region above the storage capacitor, and a buried strap formed on the first vertical edge between the storage capacitor and the transistor. An isolation collar region is formed on the second vertical edge of the trench, such that the isolation collar extends the length of the transistor. The isolation collar has a bottom edge that is vertically separated from the top surface of the trench ~~buried strap~~ by about 500 to 1000nm.

Please amend paragraph 0047 as follows:

As illustrated in Figure 2A, conventional masking or lithography techniques are used to deposit a layer of silicon nitride 24 onto undoped polysilicon surface 16 (Figure 1A). The silicon nitride 24 is deposited on both undoped polysilicon surface 16 (Figure 1A) and collar oxide regions 14. Only the doped polysilicon pads 12 (Figure 1A) are not covered with the deposited silicon nitride 24 [[12]]. As shown in Figure 2B, polysilicon regions 18 (Figure 1B) are etched down to a depth of between approximately 200-400 nm to form a recess 26 within each trench region 22.

Please amend paragraph 0053 as follows:

Following the formation of oxidized polysilicon liner 50 (Figure 7B), recess regions 26 are filled with an etch resist material 52, as illustrated in Figure 8B. Figure 8B also shows oxide layer 40 and silicon nitride layer 24 that have been deposited on the silicon surface 54 of the semiconductor material used to fabricate the vertical DRAM cells. Figure 8B is a cross-sectional view of Figure 8A taken along axis A-A', where Figure 8A shows a top view of the etch resist material 52. ~~Figure 8B is a cross-sectional view of Figure 8A taken along axis A-A'.~~

Please amend paragraph 0055 as follows:

As illustrated in Figure 10A, the etch resist material 52 filling recess regions 26 (Figure 7B) is partially etched along vertical edges 60. This creates a vertical channel opening 62 down each of the vertical edges 60 [[62]]. Vertical channel opening 62 allows further etching for generating a buried strap. The buried strap connects the transistor (not shown) and the capacitor (not shown) of a single unit cell to form a DRAM storage node within each trench region 22 (Figure 1B). As shown in Figure 10A, the areas surrounding vertical channel opening 62 that are not covered by etch resist 52 are further etched.

Please amend paragraph 0061 as follows:

In one embodiment of this aspect of the present invention, the depth of the STI region 76 is less than or equal to about 250 to 350 nm. Even more shallow depths, such as from 50 to 150nm or less, may also be desirable and within the scope of the present invention. STI region 78 provides similar isolation between cell 2 and another adjacent DRAM device (not shown). Within each cell, the lateral displacement of the buried strap 72 with respect to the

oxide collar 14 enables the oxide collar 14 to terminate roughly at or even above the buried strap 72 in the vertical direction, which allows for a shorter depth of isolation and thus a shallower trench. In one embodiment of this aspect of the present invention, the collar oxide 14 has a bottom edge extending below the vertical location of the top surface of the buried strap by about 50-100 nm and vertically separate from the top surface of the ~~buried strap~~ trench by about 500-1000 nm.